

ATS WHITE PAPER

Device Thermal Coupling on a PCB



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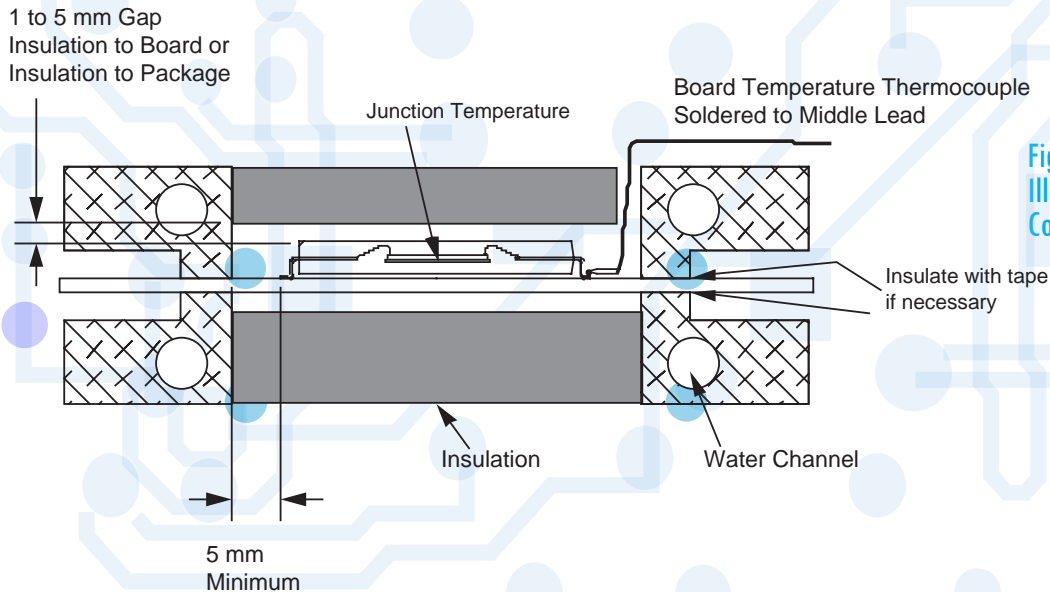


Figure 1. Cross Section Illustration of a Ring Style Cold Plate $R_{\Theta_{JB}}$ [2].

The objective of any thermal solution is to ensure that a device's operating temperature does not exceed the safe limits defined by its manufacturer. In the electronics industry, this operating temperature is referred to as the device's "junction temperature." In a processor, for example, this term literally refers to the semiconductor junction where electrical power is converted to heat.

To maintain operation, the heat must flow out of the semiconductor at such a rate as to ensure acceptable junction temperatures. This heat flow encounters resistance as it moves from the junction throughout the device package, much like electrons face resistance when flowing through a wire. In thermodynamic terms, this resistance is known as conduction resistance and consists of several parts. From the junction, heat can flow toward the case of the component, where a heat sink may be located. This is referred to as Θ_{JC} , or junction to case thermal resistance. Heat can also flow away from the top surface of the component and into the board. This is known as junction to board resistance, or Θ_{JB} .

Θ_{JB} is defined as the temperature difference between the junction and the board divided by the power when the

heat path is from junction to board only. To measure Θ_{JB} , the top of the device is insulated and a cold plate is attached to the board edge (Figure 1). This is the true thermal resistance, which is the characteristic of the device. The only problem is that, in a real application one does not know how much power is being transmitted from different paths.

Ψ_{JB} is a measure of the temperature differential when multiple heat transfer paths are used, such as the sides and top of the component as well as the board. These multiple paths are inherent in an actual system and measurements must be used with caution.

Due to the multiple heat transfer paths within a component, a single resistance cannot be used to accurately calculate the junction temperature. The thermal resistance from junction to ambient must be broken down further into a network of resistances to improve the accuracy of junction temperature prediction. A simplified resistor network is shown in Figure 2.

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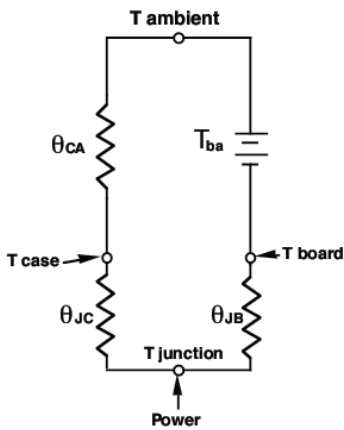


Figure 2. Junction to Ambient Resistor Network [1].

Prior work done by Joiner *et al.* correlates Θ_{JMA} to board temperature (see Equation 1). The Θ_{JMA} is the overall thermal resistance from the junction to the ambient when all heat transfer paths are evaluated. In this case, Θ_{CA} is represented by the heat sink thermal resistance, as well as the interfacial resistance between device and sink.

Table 1 lists JEDEC parameters for a typical BGA component. These are used in the following example calculation.

- Θ_{JMA} = junction to moving air thermal resistance
- Θ_{JB} = Junction to board thermal resistance
- Θ_{JC} = Junction to case thermal resistance
- Θ_{CA} = Case to ambient thermal resistance
- T_{BA} = Board temperature rise

$$\theta_{JMA} = \frac{(\theta_{JC} + \theta_{CA}) \times \theta_{JB}}{(\theta_{JC} + \theta_{CA}) + \theta_{JB}} + \frac{(\theta_{JC} + \theta_{CA})}{(\theta_{JC} + \theta_{CA}) + \theta_{JB}} \times \frac{T_{BA}}{P} \quad (1)$$

Parameter	Description	Value	Units
Θ_{JC}	Thermal Resistance - Junction to Case	0.45	$^{\circ}\text{C}/\text{W}$
Θ_{JB}	Thermal Resistance - Junction to Board	2.6	$^{\circ}\text{C}/\text{W}$
T_{DP}	Thermal Design Power	20	W
T_j	Maximum Junction Temperature	105	$^{\circ}\text{C}$

Table 1. Typical Thermal Package Specifications.

As board layouts become denser, there is a need to design optimized thermal solutions that use the least amount of space possible. Simply put, there is no margin to allow for over-designed heat sinks with tight component spacing. Accounting for the effect of board coupling is an important part of this optimization. The possibility for

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using an oversized heat sink exists only if the junction to case heat transfer path is considered.

To ensure a 105°C junction temperature at 55°C ambient a typical component (see Table 1) needs a heat sink resistance of 2.05°C/W (if we ignore board conduction). When board conduction is taken into account, the actual junction temperature could be as low as 74°C, assuming the board temperature is the same as the air temperature. This indicates a heat sink that is larger than necessary.

From this example, it is clear that all heat transfer paths from the component junction must be considered. Using just the Θ_{JC} and Θ_{CA} values can lead to a larger than optimal heat sink and may not accurately predict operating junction temperatures. Using the proposed correlation can also predict junction temperature when the board temperature is known from experimentation, as shown in Figure 3.

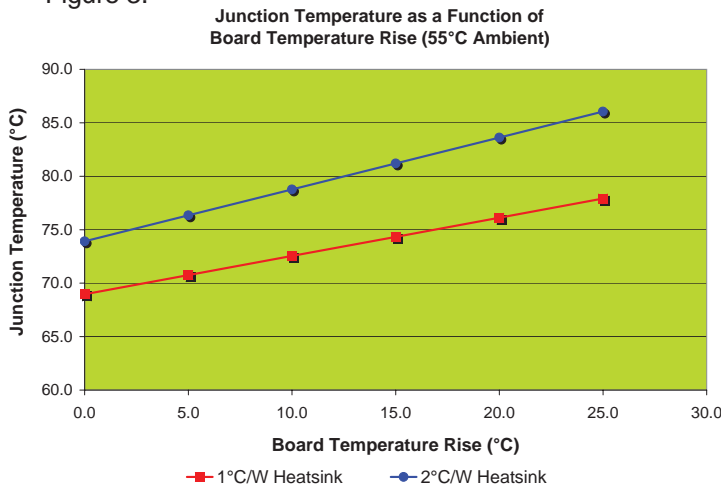


Figure 3. Effect of Board Temperature Rise on Junction Temperature.

When there is more than one component, the situation becomes much more complex than with just a single component on the board. There is conduction coupling between components through the PCB, and radiation and convective coupling between the components and adjacent cards. A simple PCB with two components is shown in Figure 4. The power dissipation of the two components is assumed to be P1 and P2, and it is assumed that we can neglect the radiation heat transfer. The board temperature under each device is T_{b1} and T_{b2} , respectively. We also assume that the lateral resistance between the two components on the board is θ_{b1b2} .

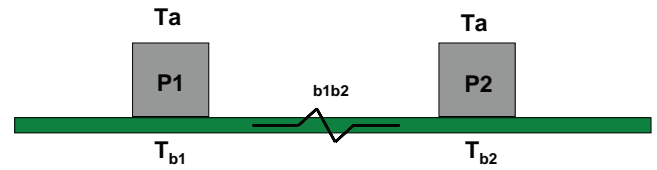


Figure 4. Simple Schematic of a PCB with Two Components.

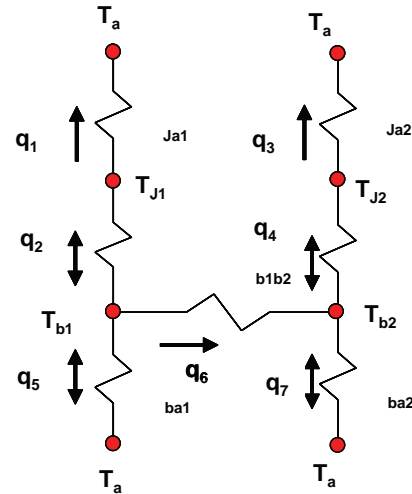


Figure 5. Simple Resistor Network of the PCB with Two Components.

Applying the energy balances at the nodes J_1 , J_2 , b_1 and b_2 :

$$\frac{T_{J1} - T_{a1}}{\theta_{Ja1}} + \frac{T_{J1} - T_{b1}}{\theta_{Jb1}} = P1 \quad (2)$$

$$\frac{T_{J2} - T_{a2}}{\theta_{Ja2}} + \frac{T_{J2} - T_{b2}}{\theta_{Jb2}} = P2 \quad (3)$$

$$\frac{T_{b1} - T_{b2}}{\theta_{b1b2}} = q_6 = q_2 - q_5 = \frac{T_{J1} - T_{b1}}{\theta_{Jb1}} - \frac{T_{b1} - T_a}{\theta_{ba1}} \quad (4)$$

$$\frac{T_{b2} - T_{b1}}{\theta_{b1b2}} = \frac{T_{J2} - T_{b2}}{\theta_{Jb2}} + \frac{T_{J1} - T_{b1}}{\theta_{Jb1}} - \frac{T_{b1} - T_a}{\theta_{ba1}} \quad (5)$$

There are four equations and four unknowns: T_{J1} , T_{J2} , T_{b1} and T_{b2} . The unknowns can be determined by solving the simultaneous equations. This simple example demonstrates that by coupling two components through a conduction path, it becomes much more complicated to find the junction temperatures. In a real life application, the situation is much more complicated than the above example when encountering multiple components and multiple PCBs with different conduction planes all inter-

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acting through conduction, convection, and radiation.

To obtain reasonable answers it is necessary for the designer to use sound engineering judgment in approximating the coupling between different components. This can be achieved by the following methods:

Method 1 - Analytical models, using either a control volume method or a resistor network model. This method requires oversimplification of the problem, otherwise the solution becomes very complicated and impractical. Method 2 - Use of CFD on a simplified geometry, as described by Guenin [4]. This method suggests that an equivalent surface area for a component is found as:

$$A_n = \frac{P_n}{P_{Total}} \cdot A_{Total} \quad (6)$$

Where A_n is the equivalent footprint area of the component, P_n is the power dissipation of the component, P_{Total} is the total power dissipation and A_{Total} is the total surface area of the PCB. After the equivalent footprint area is calculated, a simple PCB with a single component having the footprint area A_n and power dissipation of 1 Watt can be simulated using CFD. This process effectively calculates the difference between the board temperature and the ambient (θ_{BA}) for a 1 Watt power dissipation. Figure 6 shows the CFD simulation on one such component and Figure 7 shows the θ_{BA} as a function of PCB size. Figure 7 can be used to determine the θ_{BA} for other components by simply calculating their effective footprint area. It is assumed that all components have the same footprint size.

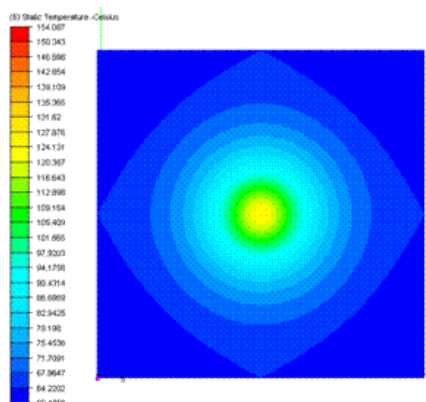


Figure 6. CFD Simulation of a Single Component on a PCB [4].

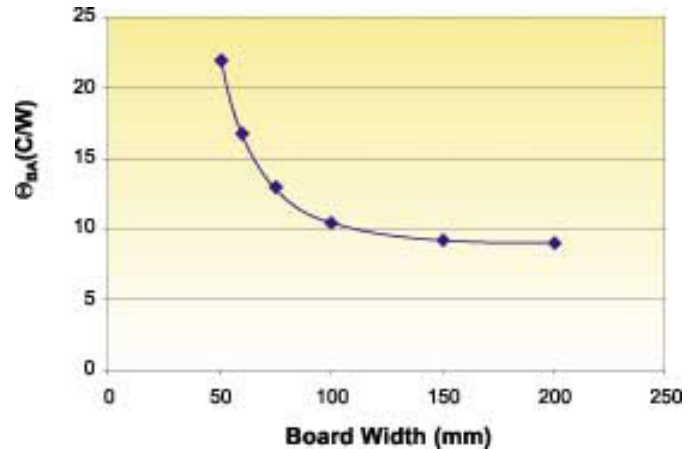


Figure 7. θ_{BA} Distribution as a Function of PCB Size [4].

The board temperature can then be calculated as:

$$T_B = P_n \times \theta_{BA} \quad (7)$$

The junction temperature can then be calculated as:

$$T_J = T_B + P_n \times \Psi_{JB} \quad (8)$$

Where Ψ_{JB} is the characterization parameter.

Method 3 - Measure the board temperature, T_B , experimentally, if the PCB is available, and use Equation 8 to find the junction temperature. Again, this is an approximation, as the conditions under which the device is coupled to the PCB might be totally different than those used with the JEDEC test board.

References:

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4. Guenin, B., Characterizing a Package on a Populated Printed Circuit Board, Electronics Cooling Magazine, May 2001