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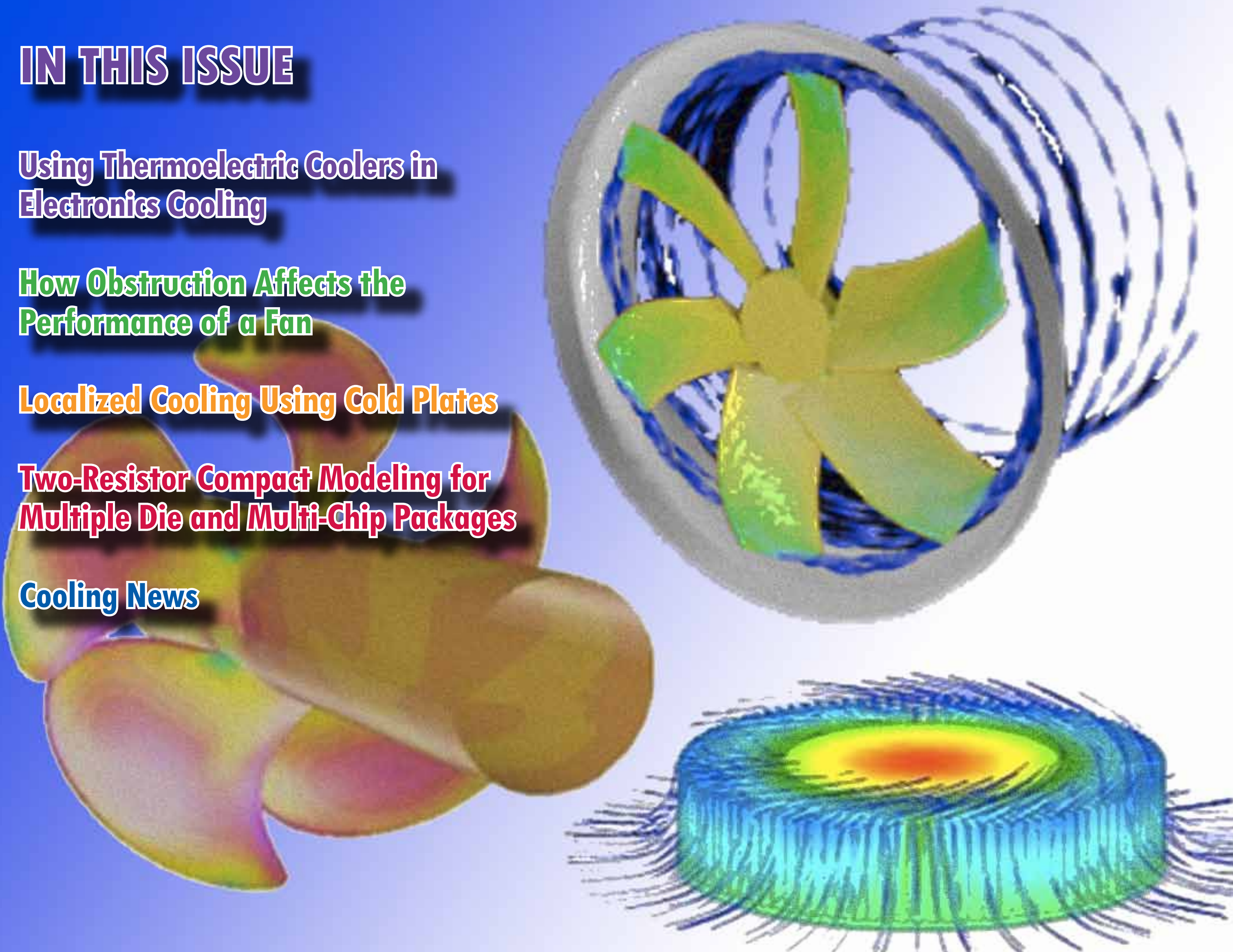
Qpedia



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Advanced Thermal Solutions is a leading engineering and manufacturing company supplying complete thermal and mechanical packaging solutions from analysis and testing to final production. ATS provides a wide range of air and liquid cooling solutions, laboratory-quality thermal instrumentation, along with thermal design consulting services and training. Each article within Qpedia is meticulously researched and written by ATS' engineering staff and contributing partners. For more information about Advanced Thermal Solutions, Inc., please visit www.qats.com or call 781-769-2800.

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Qpedia's editorial team includes ATS' President & CEO, Kaveh Azar, Ph.D., and Bahman Tavassoli, Ph.D., the company's chief technologist. Both Azar and Tavassoli are internationally recognized experts in the thermal management of electronics.

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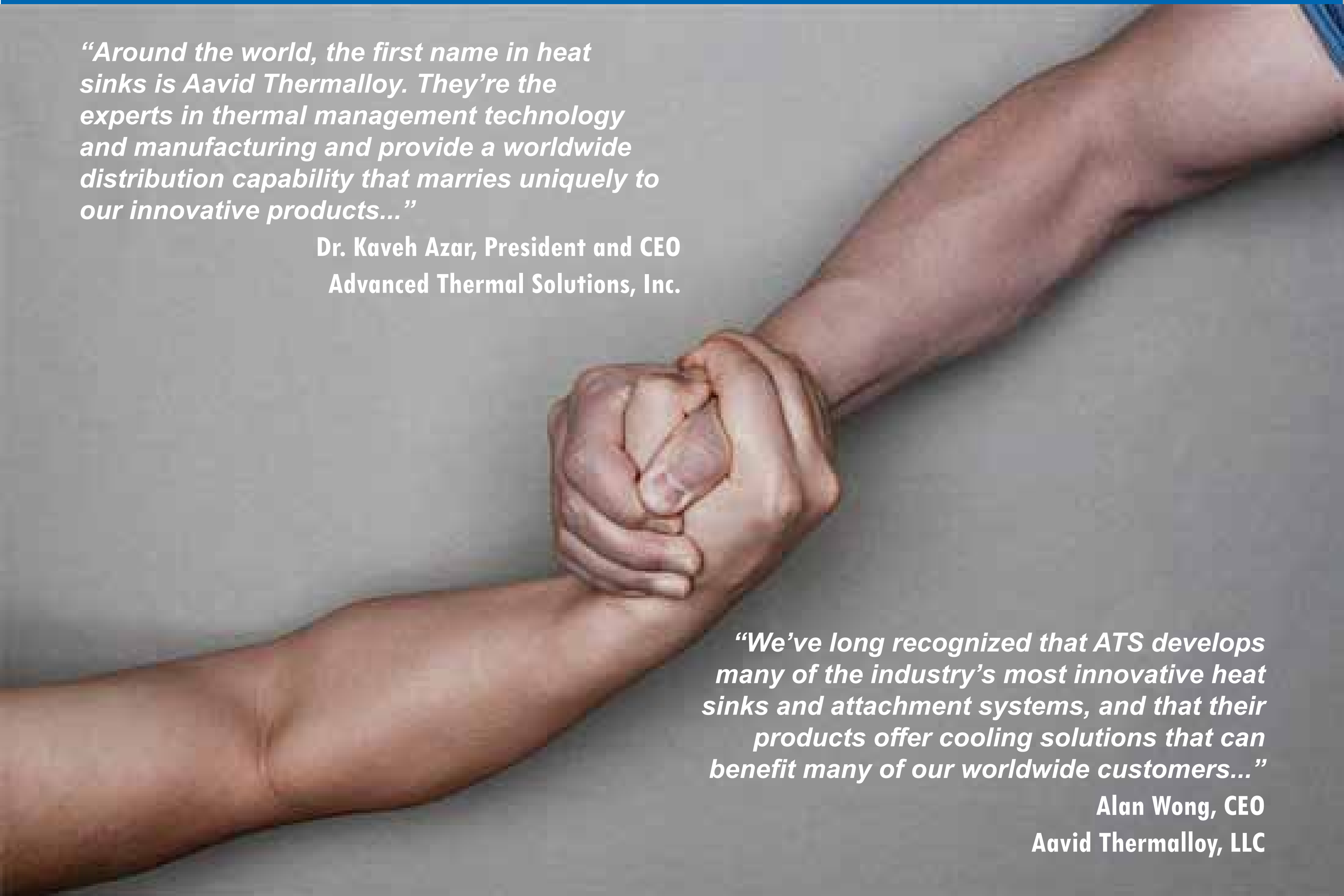
Features

TWO THERMAL MANAGEMENT POWERHOUSES JOIN FORCES



AAVID THERMALLOY TO GLOBALLY DISTRIBUTE ATS HEAT SINK AND ATTACHMENT PRODUCTS

Aavid Thermalloy, LLC, the world's oldest and one of the largest suppliers of thermal management products to the worldwide electronics marketplace, has signed a distribution agreement with Advanced Thermal Solutions, Inc. (ATS), a leader in innovative component cooling solutions. Aavid Thermalloy, with its global customer base and broad network of sales offices, representatives and distributors, will now have access to ATS' high performance heat sink and attachment technologies to address the cooling of today's and tomorrow's electronic devices.

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Using Thermoelectric Coolers

in Electronics Cooling

Thermoelectric devices are semiconductor modules which use the Peltier effect to create a heat flux between the junctions of two different types of materials. Named after French physicist Athanase Peltier, the effect shows that a temperature differential is created when DC current is applied across two dissimilar materials. (It is one of the three thermoelectric effects; the others are the Seebeck effect and Thomson effect.)

A typical thermoelectric module is manufactured using two thin ceramic wafers with a series of N and P doped bismuth-telluride semiconductor material sandwiched between them. The ceramic material adds rigidity and the necessary electrical insulation. The N type material has excess electrons, while the P type material has a deficit of electrons. One N and one P make up a couple, as shown in Figure 1.

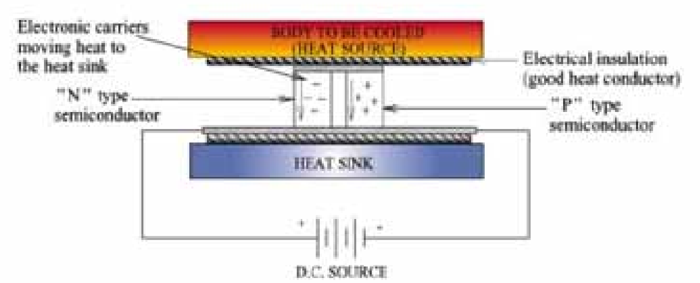

Figure 1. Illustration of a Thermoelectric Module [1].

When a DC current is applied to the circuit, the thermoelectric module can work as a cooler or heater depending on the current's direction. A thermoelectric cooler (TEC), or solid state heat pump transfers heat from one side of the device to the other side against the temperature gradient. Many products use thermoelectric coolers, including small refrigeration systems, CCD cameras, laser diodes and portable picnic coolers. They are also used in the thermal management of microprocessors, memory modules and other electronic devices. Figure 2 shows the Cooler Master V10 TEC CPU heat sink.

Figure 2. Cooler Master V10 TEC CPU Heat Sink [2].

Although a TEC provides a very simple and reliable solution for cooling devices, its poor thermal performance prevents its broader usage. Compared with traditional refrigeration systems, the coefficient of performance (COP) of a TEC is only about 1/5 that of a refrigeration system using a vapor compression cycle. Currently, the uses of TECs in electronics cooling are limited to systems that require temperature stability or sub-ambient operating conditions, or specially designed devices. Laser beam components and high energy optical modules are such examples.

Figure 3 compares a regular heat sink and heat sink with a TEC module. For the sake of simplicity, all the interfacial and contact resistances are ignored.

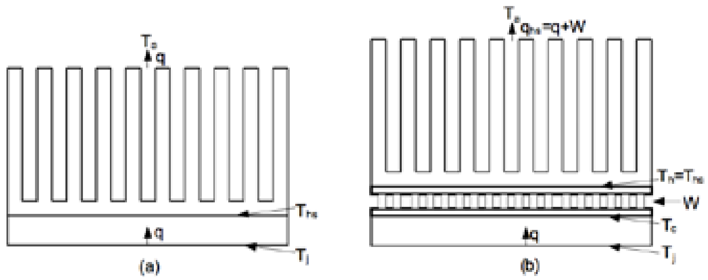

Figure 3. Schematic of (a) a Regular Heat Sink; (b) a Heat Sink with a TEC.

For Figure 3(a), the device's junction temperature can be predicted simply as,

$$T_j = T_a + (R_{jc} + R_{hs})q \tag{1}$$

Where $\boldsymbol{R}_{jc}$ is the device thermal resistance from junction to case, and $\boldsymbol{R}_{hs}$ is the thermal resistance of the heat sink from base to ambient. For the heat sink with a TEC, the junction temperature of the device is

$$T_j = T_c + R_{jc}q \tag{2}$$

Where $\boldsymbol{T}_c$ is the TEC cold side temperature.

The heat sink temperature is,

$$T_{hs} = T_h = T_a + R_{hs}(q + W) \tag{3}$$

And $\boldsymbol{T}_h$ is the TEC hot side temperature.

The COP (coefficient of performance) of the TEC for cooling is defined as,

$$COP = \frac{q}{W} \tag{4}$$

Where $\boldsymbol{q}$ is the heat removed from the cold side by the TEC and $\boldsymbol{W}$ is the electric energy consumed by the TEC.

Equation 3 can be written as,

$$T_h = T_a + R_{hs}(1 + \frac{1}{COP})q \tag{5}$$

Let

$$\Delta T_{TEC} = T_h - T_c \tag{6}$$

The junction temperature of device becomes

$$T_j = T_a + R_{hs}(1 + \frac{1}{COP})q - \Delta T_{TEC} + R_{jc}q \tag{7}$$

It can be written as

$$T_j = T_a + (R_{hs} + R_{jc})q - \Delta T_{TEC} + \frac{R_{hs}}{COP}q \tag{8}$$

Compared to the heat sink without the TEC, the junction temperature difference between them is

$$-\Delta T_{TEC} + \frac{R_{hs}}{COP}q \, .$$

Two TECs, the RC12-8 and XKLT2418 from Marlow Industries, are used in the calculation to evaluate the TEC cooling method. A Marlow TEC is shown in Figure 4. The specifications of the two TECs are shown in Table 1.

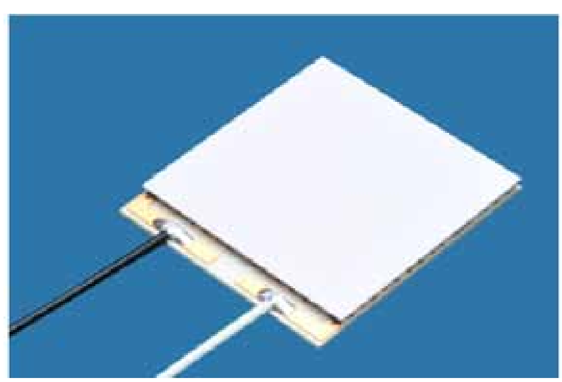

Figure 4. A TEC from Marlow Industries [3].

	RC12-8 40mm x 40mm x 3.6mm		XLT2418 40mm x 40mm x 2.3mm	
Hot Side Temperature (°C)	27	50	27	50
ΔT_{max} (°C)	66	74	56.5	64.0
q_{max} (watts)	71	78	127	141
I_{max} (amps)	7.4	7.4	13.9	13.8
V_{max} (vdc)	14.7	16.4	14.1	15.7

Table 1. TEC Specifications [3].

For the electronic device, assume the junction-to-case thermal resistance is 0.2℃/W. The thermal resistance of the heat sink is 0.2℃/W and the ambient temperature is 25℃. When the heat flux generated by device is 20W, the junction temperature for device without the TEC will be 33℃. For the device with TEC, the heat sink will dissipate both the heat generated by device and the TEC. Figure 5 shows the predicted device junction temperature for the heat sink with the TEC at different operating conditions. By using a TEC, the device junction temperature is less than the 33℃. It can also be cooled to below the ambient temperature if it is needed. The value of ΔT_{TEC} is directly proportional to the voltage applied on the TEC. The larger the ΔT_{TEC}, the bigger the voltage and energy consumed by the TEC.

Figure 6 shows the calculated COP for the TEC. Clearly the COP drops fast with the increase of ΔT_{TEC}. Figure 7 shows the total heat dissipated by the heat sink. As the device junction temperature becomes low, more heat is dissipated by the heat sink including the heat generated by the TEC. At a certain temperature, the heat created by the TEC will surpass the heat created by the device itself. Because the RC-128 is designed for low power applications and the XLT2418 is specially designed for high power applications, the RC-128 typically has better performance than the XLT2418 when the heat removed from device is fixed at 20W.

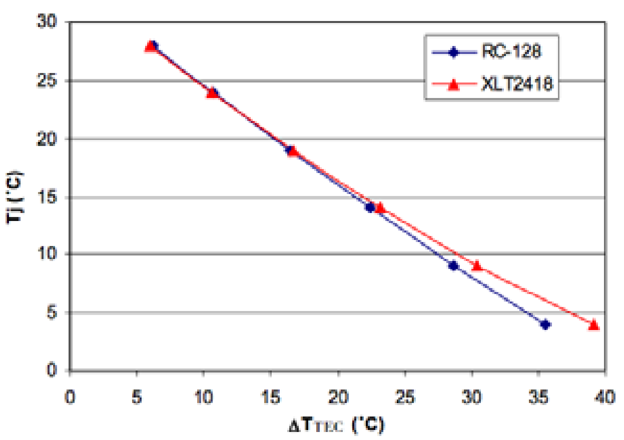

Figure 5.

T_j vs. ΔT_{TEC} ($R_{jc} = 0.2^\circ C/W$, $R_{hs} = 0.2^\circ C/W$, $q = 20W$).

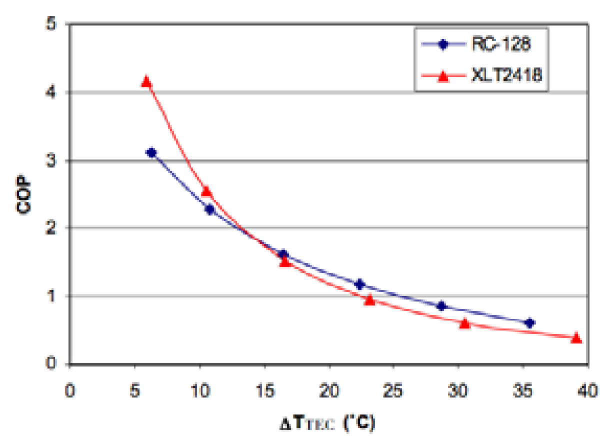

Figure 6.

COP vs. ΔT_{TEC} ($R_{jc} = 0.2^\circ C/W$, $R_{hr} = 0.2^\circ C/W$, $q = 20W$).

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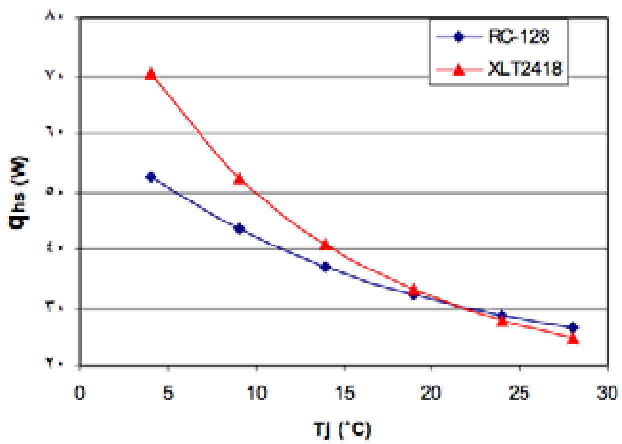

Figure 7.

q_{hs} vs. ΔT_{TEC} ($R_{jc} = 0.2^{\circ}C/W$, $R_{hs} = 0.2^{\circ}C/W$, $q = 20W$).

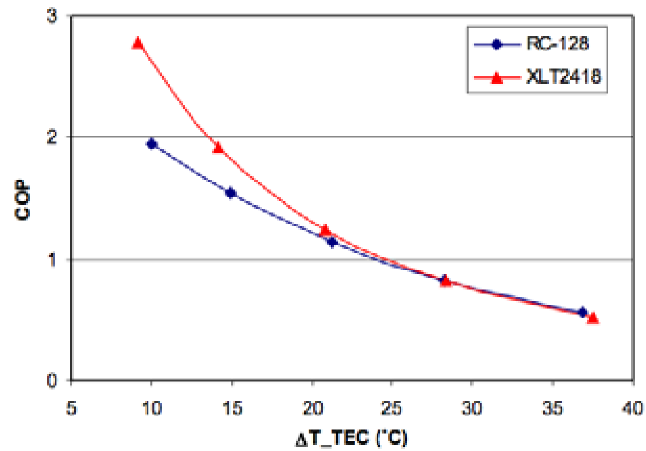

Figure 9.

COP vs. ΔT_{TEC} ($R_{jc} = 0.2^{\circ}C/W$, $R_{hs} = 0.2^{\circ}C/W$, $q = 30W$).

When the heat flux generated by the device is 30W, the device junction temperature for the heat sink without a TEC will be 37 °C. Figure 8 shows the predicted device junction temperature for a heat sink with a TEC at different operating conditions. With an increase of device heat flux, the TEC is less effective. The XLT2418 shows better performance than the RC-128 because it is designed for higher heat flux applications.

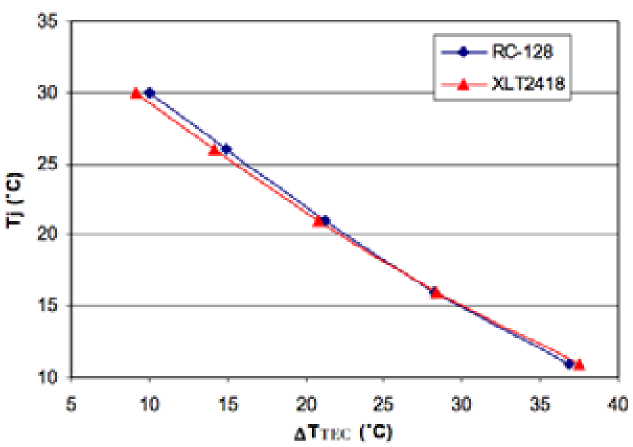

Figure 8.

T_j vs. ΔT_{TEC} ($R_{jc} = 0.2^{\circ}C/W$, $R_{hs} = 0.2^{\circ}C/W$, $q = 30W$).

Figure 9 shows the calculated COP for a TEC at 30W. When compared with the COP of a 20W case at the same junction temperature, the COP at 30W is much lower. That indicates that the TEC is less effective at higher heat flux.

From the above calculations, it is obvious that a TEC's COP decreases with an increase of heat flux and ΔT_{TEC}. TECs have limited heat transfer ability at certain TEC ΔT_{TEC} and their cooling performance worsens as heat flux approaches that limit. If TEC the COP is too low, more waste heat will be generated by the TEC, which will put a heavy burden on the heat sink and increase its temperature. Increasing the heat sink temperature will degrade the TEC's performance even more.

The device junction temperature T_j is also affected by a heat sink's thermal resistance, as demonstrated in Equation 8. This is because the heat generated by a TEC must be dissipated to ambient through the heat sink.

In cooling applications where TECs are used, it is important to comply with the following design rules:

1. Use a TEC at the operation point where the heat flux is much less than its maximum heat flux.

2. Optimize the design to decrease ΔT_{TEC} to allow better COP.

3. Use a high performance heat sink.

4. Use active temperature control, which will reduce the temperature swing.The cooling system will also last longer and save more energy in a long run.

The electric and thermal performance of current TECs is still low compared with other refrigeration methods. Researchers in physics and material science are actively looking for new materials and packaging methods to improve TECs' efficiency. With advances in technology, TECs will find more applications in electronic cooling in the future.

References:

1. http://www.melcor.com/tec_intro.html
2. http://www.coolermaster-usa.com/
3. http://www.marlow.com/

How Obstruction Affects

the Performance of a Fan

Despite continued increases in power dissipation and the growing rush to deploy liquid cooling, air cooling remains the preferred method for thermal management of electronics. Air movers, commonly called fans, play a pivotal role in air-cooled electronics. They are also an essential component of a liquid-cooled system. Proper performance of the fan, irrespective of its type, is the corner-stone of a cooling system. Yet, as engineers are designing such systems, or when systems with fans are deployed on premises, it is common that little attention is given to the placement of the fan or to objects in its vicinity. Thus, the fans tend not to work at their optimum stages.

and subsequent distribution is critical to fan performance. Figure 1 demonstrates the flow distribution that is created on the blade and across the fan as the result of the blades' shape and rotation speed.

The more aerodynamically efficient the design of the fan blades and hub, the better is the performance of the fan. When we refer to performance, we are talking about a fan that has the highest volumetric flow rate, at the lowest pressure drop for the least energy consumed. Therefore, anything we do to the fan design or its deployment that can adversely impact the flow structure around the blade, will adversely impact fan performance.

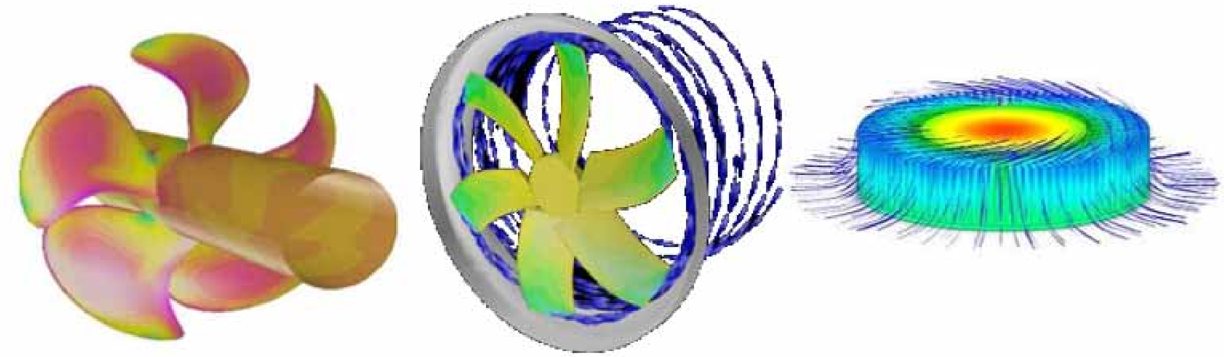

Figure 1. Flow Distribution On and Across Three Fan Types.

Previous articles in Qpedia have covered different facets of a fan's operation and deployment in electronics systems, [1, 2, and 3]. Here we explore the impact of obstruction on the performance of a fan deployed for bulk air movement within a system or in a facility such as a data center.

The basic premise for understanding fan operation is to clearly know the role of the blades in creating a pressure differential, which thus creates the fluid flow across the fan opening. Regardless of the fan type, the blades' flow creation

The literature is rich with such studies because fans have been exhaustively deployed across various industries. One broadly used reference is highlighted in [4]. The following areas are considered deployment circumstances that will affect fan performance:

1. Elbows
2. Sharp-edged entrance
3. Swirling flow at the inlet
4. Obstruction at the inlet
5. Fan within a cabinet

Elbows

Elbows close to the fan inlet cause non-uniform distribution of air. This results in flow starvation for part of the blade. Figure 2 shows the effect of an elbow on fan performance.

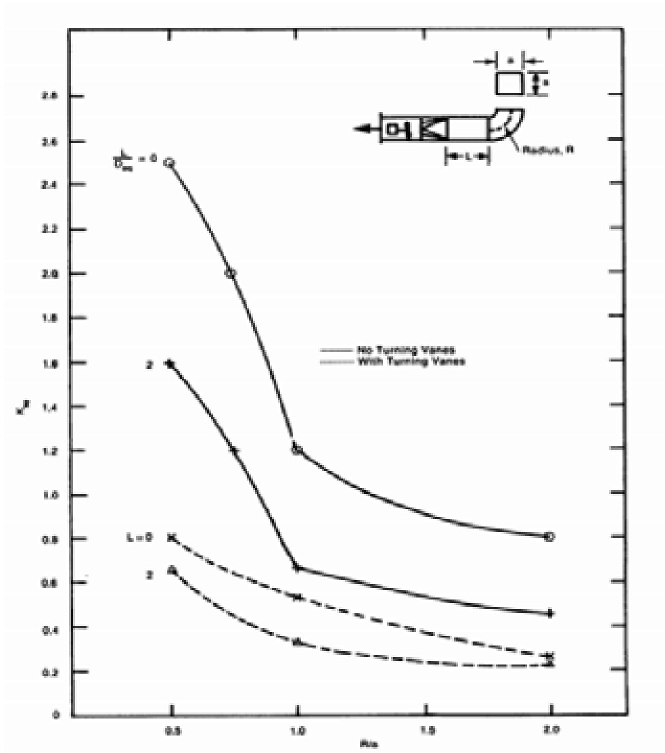

Figure 2. System Effect Coefficient for a Square Elbow at Fan Inlet [4].

Where R is the radius of the elbow and the "a" is the size of the square duct. To calculate the pressure drop as the result of the elbow, the following equation is used:

$$\Delta P = 1/2 V^2 K_{se}$$

Where K_{se}, the system effect loss coefficient, is obtained from Figure 2 for a given R/a., Elbows are not used in most electronics applications. However, in many chassis, designers have used vane-like elbows to provide uniform flow to the card array.

Sharp-edged Entrance

The flow into a sharp-edge orifice causes the formation of vena contracta, the narrowest point in a fluid stream. The result is a loss of flow area. Fans without inlet duct connections, for example those directly mounted into a plenum, should be provided with a rounded entry. Otherwise, a loss in performance will occur due to the reduction in inlet flow area.

Swirling Flow at the Inlet

The fan intake design may cause swirling flow. If the direction of the swirl is the same as the blade, it affects upstream pressure, hence it decreases fan effectiveness (decreases the pressure). If the swirl is in the opposite direction against the blade rotation, it requires more power consumption by the fan to reach the same performance.

Obstruction at the Inlet

Any obstruction at the inlet will result in a reduction in the flow area. Therefore, it will affect the performance of the fan. The magnitude of impact is directly correlated to the size of the obstruction. The following figure shows its impact on the value of K_{se}.

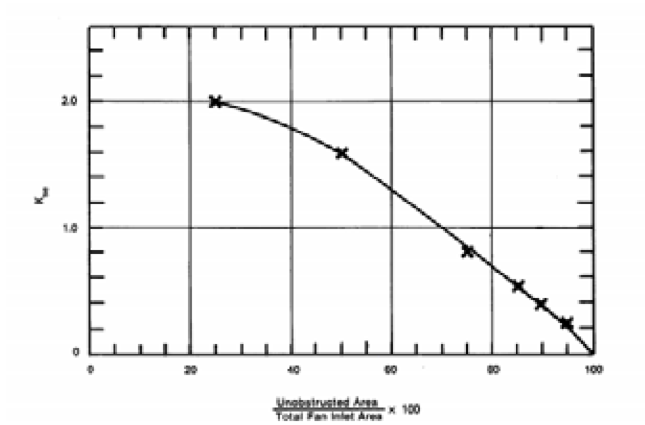

Figure 3. System Effect Loss Coefficient for Fans with Obstructed Inlets as a Function of Unobstructed Area/Total Fan Inlet Area [4].

The relationship between K_{se} and area ratio, shown in Figure 3 clearly suggests the negative impact on the pressure drop with the increase of the obstruction. Since it is very difficult to design a system without any obstruction, the data shows that a well designed area will have a K_{se} of less than 0.6.

Fan within a Cabinet

Fans within cabinets should be located to permit unobstructed flow into the inlet area. Loss in performance will occur otherwise. The K_{se} coefficient can be calculated as follows:

$$K_{se} = 0.16(\text{fan inlet diameter/distance of fan inlet from wall})^{1.25}$$

The distance between the fan inlet and a wall should be at least 0.6 times the impeller diameter. If two centrifugal fans are in one cabinet, their inlets should be at least 1.2 times the impeller diameter apart.

The relative position of the cabinet inlet and fan inlet should be such that it does not cause rotation of air at the fan inlet. It is obvious that as we design cooling systems for our electronics, the details required to facilitate the entry of air to the fan systems must be a point of concern. Often, details associated with the system site implementation, cabling, baffles, adjacent systems, etc. are major contributors to the successful operation of the air movers within electronic systems. System internal design, with respect to the fans and their locations, play a pivotal role in their operations. Depending on the location of the air-mover system within a chassis, there are a number of components such as air filters, card guides, memory and daughter cards, fuses and power delivery circuits that will adversely affect the operation of the air-movers.

We have often done full testing of products in our labs and chambers, yet we hear from our customers that our fully tested system is not functioning properly. This is despite the fact that testing showed that the system meets the stated requirements. Yet, we discover that the system was deployed in such a manner that subtle obstructions, such as cabling or system placement, are actually restricting the performance of the air-movers.

On the system placement, one of the most common occurrences is that the system is placed in a high-velocity air flow such as the exhaust of the building's HVAC diffuser. On the surface, it appears that the system is engulfed in a high speed air flow and therefore must perform better thermally. But what we may not pay attention to is that the high speed air from the HVAC system is altering the pressure distribution across the air-movers within the system, thus reducing their ability to circulate the air within the system. A successful design will encompass all such issues and explore their likely occurrences. A solution should be designed and tested under all possible circumstances before the product is launched.

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2. Using Fan Trays in Electronic Systems Qpedia Thermal E-Magazine, July 2008.
3. How Baffles and Plenums Affect Fan Performance, Qpedia Thermal E-Magazine, April 2009.
4. Fluid Flow Data Book, Genium Publishing Corp., Schenectady, NY, 1984.

CLWT-067

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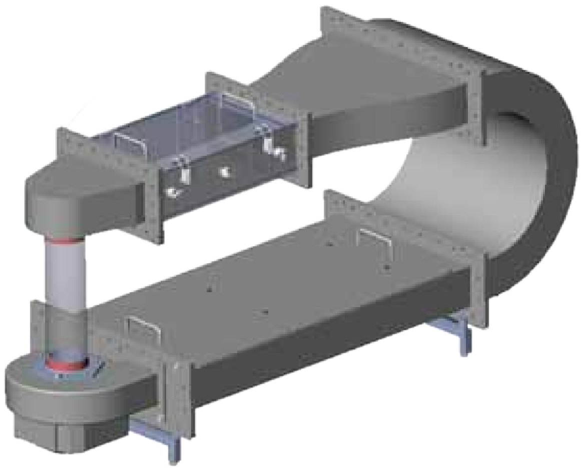

The CLWT-067 is a research-quality closed loop wind tunnel that provides a convenient, accurate system for thermally characterizing PCBs and individual components at controlled temperatures from ambient to 85°C.

The CLWT-067 wind tunnel produces air flows up to 7.5 m/s (1500 ft/min). With customization, it can generate flows up to 50 m/s (10,000 ft/min) using orifice plates (available optionally). The clear Lexan test section lets the user to view the test specimen and allows for flow visualization.

Unlike open loop wind tunnels, the CLWT-067 re-circulates internal air. This allows the system heater to quickly warm the air to a specific temperature. The testing of boards and components in hot air is a requirement in some NEBS and other standards. The precise controls and temperature range of the CLWT-067 wind tunnel allows its use for testing heat sink performance and for calibrating air and temperature sensors.

The complete wind tunnel fits on most lab benches and is powered from standard AC outlets. It has a smaller footprint than traditional, closed loop wind tunnels or environmental test chambers.

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Localized Cooling

Using Cold Plates

Many applications in electronics cooling require a cold plate to remove heat from discrete components laid out on a board. In these circumstances, it is more efficient that the liquid does not completely fill the cold plate, but is only transferred to areas that need to be cooled. With this kind of design, the required volumetric flow rate of the coolant will be significantly lower than if the entire cold plate was filled with liquid. The schematic for a typical example of this scenario is given in Figure 1 [1]

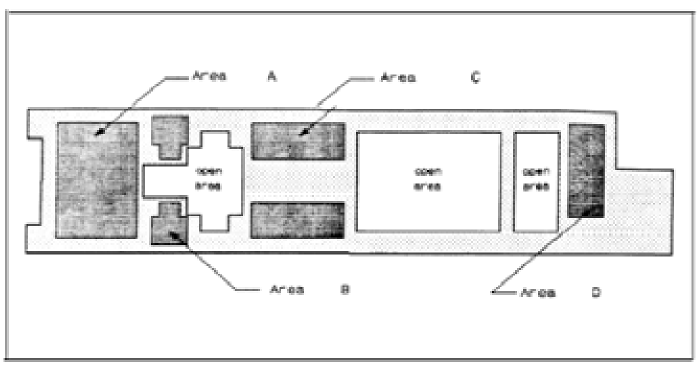

Figure 1. Schematic of a Board with a Localized Area of Heat Dissipation [1].

In Figure 1, areas A, B, C and D must be cooled for the components dissipating from 5 to 15 W/cm^2. The other areas, designated as open, have components that interfere with the cold plate and must be avoided in the design. Two designs were considered for this case: a drilled hole and a press-fit tube. Figure 2 shows the drilled hole concept. As can be seen, there are multiple small holes around the heat dissipating components under the cold plate surface. Large holes are machined to interconnect the smaller holes. A technique called gun drilling was used for machining the long holes. The entire cold plate was made from a copper block.

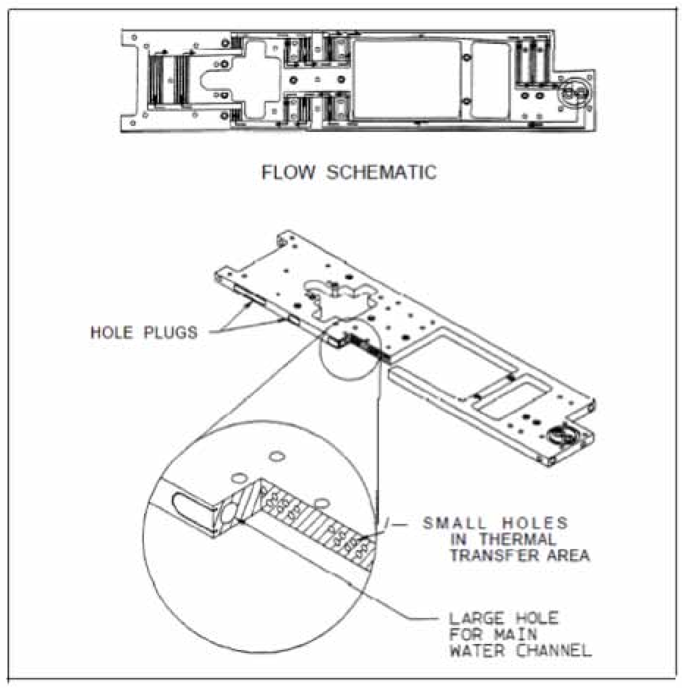

Figure 2. Schematic of the Drilled Hole Cold Plate Design [1].

Figure 3 shows the press-fit tube design. In this approach, a copper tube with high thermal conductivity is routed through the areas of heat transfer and either brazed or epoxied to the aluminum cold plate base. This design is considerably lighter and cheaper than the drilled hole design.

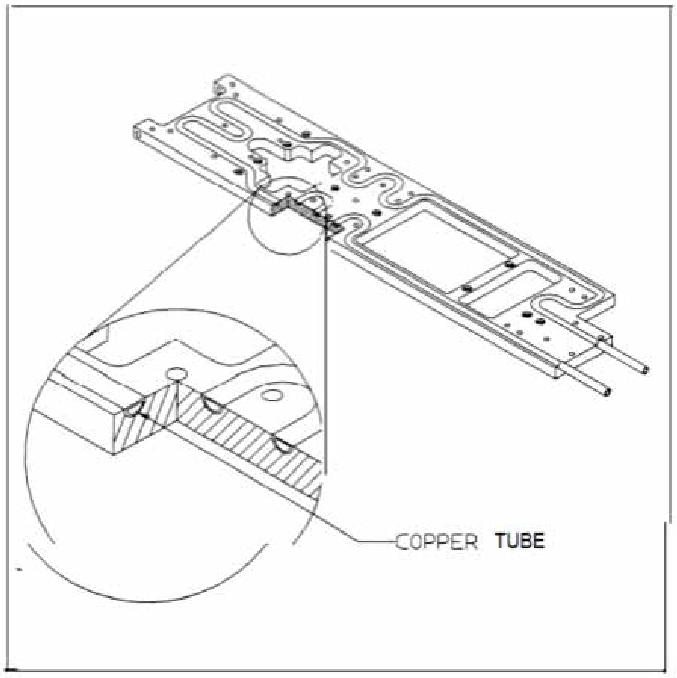

Figure 3. Schematic of the Press-Fit Tube Cold Plate Design [1].

To analyze the performance of this cold plate configuration, simple analytical tools can be used for a standard cold plate design. A brief summary of the equations is described here. To analyze the problem, we first have to calculate how much flow is going through the cold plate, and evaluate the pressure drop of the flowing fluid.

Pressure drop is calculated from:

$$\frac{\Delta P}{\rho U_m{}^2/2} = f\frac{A_{wet}}{A_c} + \sum K$$

Where

U_m = bulk mean fluid velocity (m/s)

f = fanning friction factor

A_{wet} = wetted surface area of the tube

A_c = cross section of the tube

K = loss coefficients related to turns, sudden expansion and contraction, etc.

The friction factor was obtained from the following equation which is in satisfactory agreements for the laminar, turbulent and transition regimes [2]

$$\frac{2}{f} = \left[\frac{1}{\left[(8/Re)^{10} + (Re/36500)^{20}\right]^{1/2}} + [2.21\ln(Re/7)]^{10}\right]^{1/5}$$

Where

$$Re = \frac{U_m D_h}{\nu}$$

$$D_h = \frac{4A_{wet}}{P}$$

Where ν is the kinematic viscosity of the fluid (m^2/s) and P is the wetted perimeter of the tube.

For the heat transfer calculation, the Nusselt number can be calculated from standard correlations in the literature for fully developed flow. The Nusselt number is related to the heat transfer coefficient as:

$$h = \frac{K_f.Nu}{D_h}$$

Where

K_f = fluid conductivity

For thermally developing flow the following correlation can be used [3]:

$$\frac{Nu_m}{Nu_\infty} = 1 + \frac{0.68 + 3000/Re^{0.81}}{(L/D_h)^{0.9}Pr^{1/6}}$$

Where

Nu_m = mean Nusselt number

Nu_∞ = fully developed Nusselt number

L = duct length

Then the convective resistance can be calculated as:

$$R = \frac{1}{h_m A_{wet}}$$

Where

h_m = mean heat transfer coefficient

For the tube fitted design the overall thermal resistance is made of four components: convection, tube conduction resistance, epoxy conduction resistance and the cold plate. It is stated as:

$$R = R_h + R_{tube} + R_{epoxy} + R_{coldplate}$$

Where

R_h = convection resistance

R_{tube} = conduction resistance of tube walls

R_{epoxy} = conduction resistance of the epoxy

$R_{coldplate}$ = conduction resistance of the cold plate

For the drilled design the overall thermal resistance can be written as:

$$R = R_h + R_{coldplate}$$

If the heat transfer coefficient is based on the local fluid temperature, then a caloric resistance must be added based on the fluid mass flow rate. The effective heat transfer coefficient is then:

$$h_{eff} = \frac{\dot{m}C_p\left\{1 - \exp[1/(R\dot{m}C_p)]\right\}}{A_{wett}}$$

Where

$\dot{m}$ = mass flow rate (kg/s)

Cp = fluid heat capacitance (kJ/kg·K)

Figure 4 shows the pressure drop of the two designs as a function of water flow rate. It can be seen that with a water flow rate up to 1.89 l/min (0.5 GPM) the pressure drop between the two designs is almost the same, but at higher flow rates the drilled design's pressure drop exceeds the tube design. The sharp 90 degrees turn of the drilled holes which lead to a higher loss coefficient is the major contributor to the higher pressure drop.

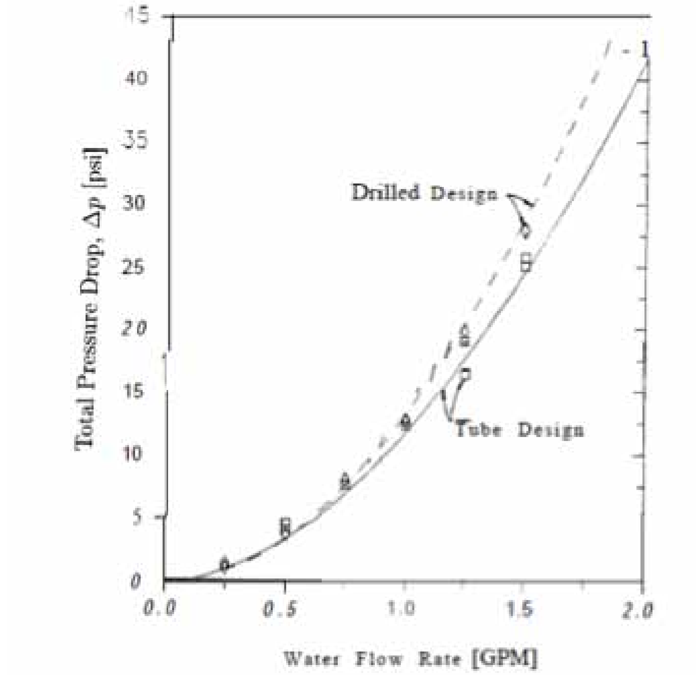

Figure 4. Total Pressure Drop of the Drilled Design and the Tube Design as a Function of the Volumetric Flow Rate [1].

Figures 5 and 6 show the effective heat transfer coefficient of the two designs as a function of flow rate. The bend and sharp increase of the curves around 0.95 l/min (0.25 GPM) is due to the flow transitioning from laminar to turbulent. The drilled hole design shows effective convection heat transfer between 7000 and 27000 W/m²K for the range of flow between 0 and 7.56 l/m (2.6 GPM). The press-fit tube design on the other hand shows a lower effective heat transfer coefficient of between 6000 and 17000 W/m²K. This is mostly due to the interfacial resistance and tube wall conduction. In the drilled design example, these two resistances do not exist. In a real application, the pumping of fluid is constrained by the pump and its characteristic curve. Even though the drilled hole shows a higher heat transfer coefficient for the same flow rate, the extra pressure drop caused by the drilled design may have a lower flow rate hence lowering the heat transfer coefficient.

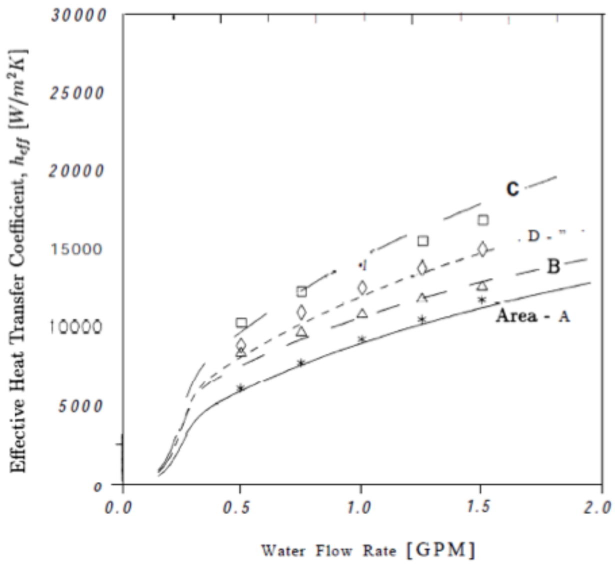

Figure 5. Effective Heat Transfer Coefficient of the Tube Design as a Function of Flow Rate for Different Regions on the Plate [1].

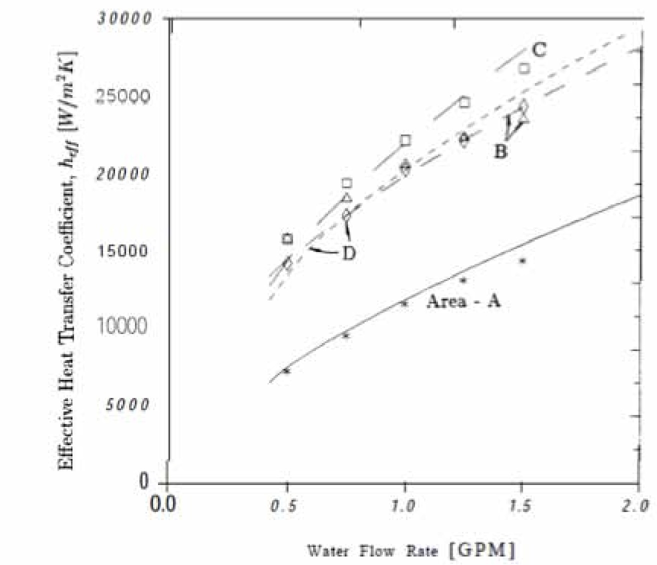

Figure 6. Effective Heat Transfer Coefficient of the Drilled Hole Design as a Function of Flow Rate for Different Regions on the Plate [1].

Figure 7 shows another cold plate design, this one by Lytron [4]. In this design, the extended-surface cold plate material and micro-channel aluminum extrusion are sandwiched between aluminum sheets. The entire assembly is welded using vacuum brazing. It is all aluminum, which makes it very light weight. The flexibility of this design allows the placement of cooling channels in different positions to enable localized cooling.

Figure 7. Lytron Vacuum Brazing of a Cold Plate for Localized Cooling [4].

The above analytics show that the performance of a cold plate for localized cooling can be calculated using a simple analytical tool. The designer then has to consider such factors as weight, manufacturing, cost and thermal performance to decide the best option for his or her design. The characteristic of the pump has a paramount effect on the design and cannot be neglected.

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4. http://www.lytron.com

Two-Resistor Compact Modeling

for Multiple Die and Multi-Chip Packages

Introduction

The two-resistance compact model is a useful method for simulating a package. Its attractiveness for an analyst is that there is no need to model the complex 3D details of the package; it is simple and intuitive. For a manufacturer, compact models conceal details for proprietary reasons. However, the challenge in the derivation of two-resistor models comes from the complexity brought about by multiple die junctions, power and thermal resistances. There is also a trend to use stack-die packages and stack-package technologies to increase the capacity and capability of electronic devices. This article will present an analysis of two-resistance compact models for the prediction of the thermal performance of a stack-die package. The method presented can also be applied to a stack-package.

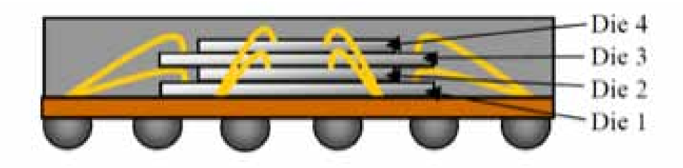


Figure 1. Typical 4-Die Stacked Chip Scale Package (SCSP) [1].

A typical stacked chip-scale package (SCSP) is illustrated in Figure 1. The die surface covers around 70% of the package area and the dies are enclosed in a low-conductivity mold compound material [1]. A major challenge for the derivation of two-resistor models for these packages comes from successive die-die adhesive layers. When calculating the thermal resistances in stacked-die packages, the critical die junction may shift between the dies in the stack depending on the amount of power applied, the environment or heat flow conditions and the sizes of the dice [1]. There will be as many thermal resistance values as there are die junctions to reference in the stack.

Methodology

Junction-to-case (θ_{jc}) and junction-to-board (θ_{jb}) thermal resistances were experimentally obtained as per the JEDEC JESD51-2 [2] and JESD51-8 [3] guide for mono-packages, respectively. These values are used as validation data for the detailed thermal model. Detailed thermal models and the various environments were generated in a computational fluid dynamics (CFD)-based software tool. Radiation calculation was done for the still-air environments by applying the appropriate emissivity and view factor for radiating surfaces. A laminar flow was assumed for air circulation around the package. For the junction-to-case environment, a cold plate was created directly on top of the package case and maintained at 25°C. Perfect insulation was placed around the package and adiabatic condition around the calculation domain walls was maintained to ensure majority of heat flow towards the case. Figure 2 shows the junction-to-case quarter model.

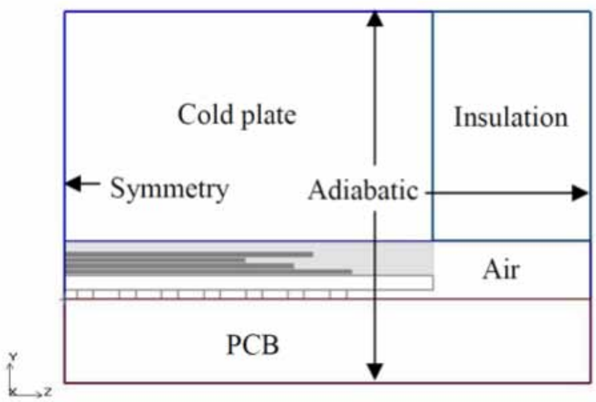


Figure 2. Side View of the Junction-to-Case (θ_{JC}) Quarter Model Showing the Package, Cold Plate and Insulation Block [1].

In the detailed model, thermal resistances were calculated from each die junction based on the relation:

$$\psi_{jxy} = \frac{T_{jx} - T_y}{P_t}$$

Where
x = 1, 2, 3 or 4 for die designation
y = a for ambient
= b for board
= c for case
P_t = Total power going through Section A

For example, for die number one the junction-to-ambient thermal resistance is ψ_{j1a}. Similarly, for the second junction it is ψ_{j2a}. The highest thermal resistance value is then referred to as ψ_{ja_max}.

Stacked-Die Package Detailed Models

For this article, a semi-detailed 3D model with typical four-die stacked-package dimensions, shown in , was used as a baseline for comparison with the compact models [1]. The 3D model contained blocks of the four dies, adhesive layers and solder balls as discrete elements. The only lacking details are the gold bond wires, and copper traces and vias in the substrate and PCB, thus neglecting the effect of heat flow through the bond wires and vias. Figure 3 shows the layout of the solder balls of the package.

The PCB and substrate bulk properties were calculated based on PCB dimension defined in JESD51-9 [4] and commercial substrate dimensions [1]. To account for better heat conduction in the copper layers, the substrate layers were treated as a resistance network as shown in Figure 4. Effective thermal conductivities are calculated in the normal direction and along the substrate plane by using Equations (2) and (3) below, respectively.

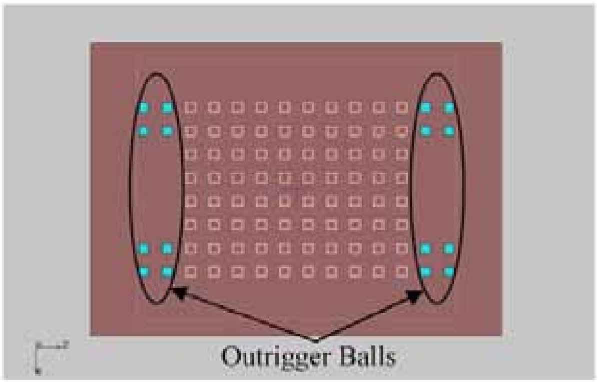


Figure 3. Bottom View of the SCSP Model Showing the Solder Balls and Their Layout. The Package Outline is Shown in Green and Outrigger Balls are Highlighted [1].

The assumed material and attribute properties are summarized in tables 1 and 2. A uniform power of 0.3 Watt applied to the top surface of each die was assumed in the study.

Parameter	Value
Mold cap	0.65 mm
4-layer BT substrate	0.28 mm
Ball height	0.27 mm
Die thickness	0.076 mm
Die-attach bond line	0.032 mm
Package body size	10 mm x 14 mm
Die 1 Size	8.8 mm x 10.9 mm
Die 2 Size	6.8 mm x 8.7 mm
Die 3 Size	5.8 mm x 6.8 mm
Die 4 Size	3.9 mm x 9.4 mm
Solder ball diameter	0.35 mm
Total solder ball count	96
Outrigger solder balls	16
Solder ball pitch	0.8 mm
Overall package thickness	1.20 mm

Table 1. Assumed Physical Dimensions for the SCSP Detailed Model[1].

$$k_{ep} = \frac{\sum k_x \delta_x}{\delta_t} \quad (2)$$

$$k_{en} = \delta_t \Big/ \sum \frac{\sigma_x}{k_x} \quad (3)$$

Component	Thermal conductivity [W/m·K]
Die	120.0
Die attach adhesive	0.9
Mold compound	0.63
Solder ball	50.2
Substrate bulk property, normal value	0.5
Substrate bulk property, in-plane value	57.7
PCB bulk property, normal value	0.6
PCB bulk property, in-plane value	46.5
Air	0.0261

Table 2. Material Property Assumptions for the Detailed Model [1].

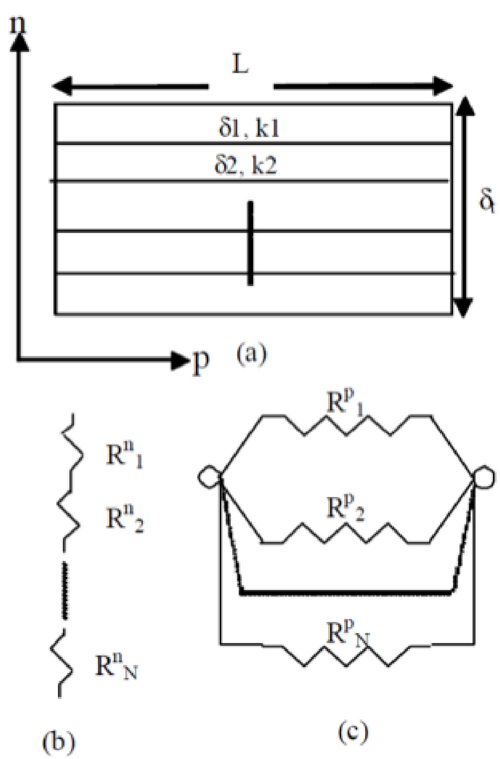


Figure 4. Schematic of Resistances in the Substrate Layers [1].

Heat transfer through radiation was included in the analyses under still-air environments, because it is known to have significant effect under this condition. The majority of the heat flow of radiation in chip-scale packages is through the top case owing to their thin profile and minimal gradient over the surface. A simplified approach is to use only the top of the case and the PCB surfaces as the radiating surfaces. Table 3 lists the emissivity values and view factors used for the models.

Component	Emissivity	View factor
Mold cap (high side)	0.95	1
PCB (high side)	0.8	0.9941
PCB (low side)	0.8	1

Table 3. Emissivity and View Factor Assumptions for the Radiation Calculation [1].

Detailed Model Results and Validation

The junction-to-ambient and junction-to-board thermal resistances were experimentally obtained. These are used to validate the assumptions made in the detailed thermal models. Experimental data obtained from measurements showed excellent correlation with the model results as shown in. The junction-to-case thermal resistances also showed excellent agreement. It is notable that the temperatures between the dies do not vary significantly. The maximum junction temperature is only around 1°C higher than the minimum value. Radiation had to be used in the junction-to-ambient model in order to get good results.

	Model results		Experimental results	
Attribute	θ_{JA}	θ_{JB}	θ_{JA}	θ_{JB}
T_{j4} [°C]	66.7	55.4	66.6	54.6
T_{j3} [°C]	66.5	55.2	66.3	54.3
T_{j2} [°C]	66.1	54.8	65.7	53.8
T_{j1} [°C]	65.6	54.3	65.1	53.1
$T_{j\ max}$ [°C]	66.7	55.4	66.6	54.6
T_a [°C]	25.2		25.5	
T_b [°C]		28.8		28.8
$\psi_{jx\ max}$ [°C/W]	34.6	22.2	34.3	21.5

Table 4. Thermal Resistances and Temperatures Obtained from the Detailed Model and Laboratory Measurements [1].

Stacked-Die Package Two-Resistor Models

The block-and-plate method was used to create the two resistor model for the stacked-die CSP in 3D space [1]. An isothermal block with thermal conductivity of 1000W/m·K was used o represent the junction node, although values of 180 and 390 W/m·K have been used without any difference in the temperatures or thermal resistances obtained. The fusion of the stacked dies into a single junction block did not show any significant changes in thermal behavior because of the notably small difference between junction temperatures of the four dies in the detailed model. Likewise, junction block thicknesses from 0.3 to 1.5 mm did not show significant differences in the results. The total package height was maintained, however, and good thermal contact between the dies was assumed. When the thermal contact is high, thermal resistances may rise significantly and the θ_{JB} and θ_{JC} predictions from the detailed model are not valid metrics for the 2R model. Here, the detailed model results are the baseline for comparison with 2R models because validation has already demonstrated the accuracy of the models.

A uniform power of 1.2 Watts was applied to the junction block, which is equivalent to the sum of the power in each die in the detailed model.

θ_{JB} and θ_{JC} values from the detailed model were applied to the resistance plates at the bottom and top of the junction block as shown in Figure 5. The thermal resistances are applied as contact resistance in the plates, either by direct input of the resistance values or by calculating the equivalent thermal conductivity from the relation:

$$k = \frac{l_p}{\theta_{JX} A}$$

Where l_p is the thickness of resistance plates.

Another isothermal block was added at the top of the θ_{JC} resistance plate to serve as case node for case temperature determination [1]. The total height, length and width of the blocks were made to equal those of the detailed package model to ensure that they have the same effect to the surrounding airflow as the detailed model.

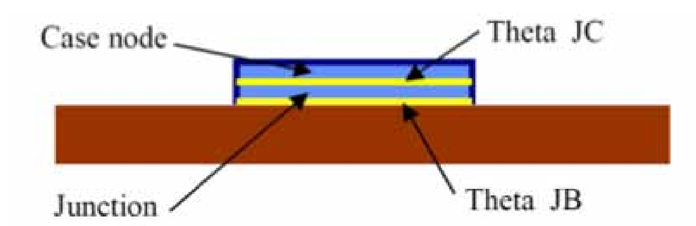


Figure 5. Two-Resistor Model Representation [1].

The case node block was found to be a key element in the model not only for determining case temperature but also for replicating heat transfer towards the case in the θ_{JA} and θ_{JC} environment [1]. Like the junction block, the case block was assigned a high thermal conductivity to minimize heat flow resistance through the block.

Comparison of the detailed and two-resistance model results in θ_{JA}, θ_{JB} and θ_{JC} are shown in and Tables 5 and 6 [1]. Results showed that the two-resistor models gave very close temperatures and resistances to the detailed model with errors of less than 5% in θ_{JB} and 0.6°C/W difference in calculated θ_{JC} values. Except in the mock-up environment, results are slightly conservative making them appropriate for quick estimates.

Attribute	θ_{JB}		θ_{JC}	
	Detailed	2R	Detailed	2R
$T_{j,max}$ [°C]	55.4	56.7	30.9	29.9
T_b [°C]	28.8	29.0		
T_c [°C]			25.2	25.0
$\psi_{Jx,max}$ [K/W]	22.2	23.1	4.7	4.1

Table 5. Comparison of the θ_{JB} and θ_{JC} Values for Stacked Die Detailed Chip Scale Package and Two Resistance Models (2R) [1].

Attribute	No radiation		With Radiation	
	Detailed	2R	Detailed	2R
$T_{j,max}$ [°C]	76.2	76.7	66.7	66.8
T_a [°C]	25.4	25.5	25.2	25.2
$\psi_{Ja,max}$ [K/W]	42.3	42.7	34.6	34.7

Table 6. Comparison of the θ_{JA} Values for Stacked Die Chip Scale Package.

Conclusions

This article has shown that the two-resistor model can be effectively used to represent stacked-die chip-scale packages with reasonable accuracy. Chip-scale packages have inherently small thermal gradients due to their large die-to-package size ratio and the fairly low thermal resistance between the die stack, making them very suitable for two resistance thermal model representation [1]. Further study is warranted to determine the range of die and package sizes at which accuracy is still acceptable.

References:

1. Garcia, E. and Chiu, C., 21st IEEE SEMI-THERM Symposium, 2005.

2. EIA/JEDEC Standard: JESD 51-2, Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air), December 1995.

3. JEDEC Standard: JESD 51-8, Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board, October 1999.

4. EIA/JEDEC Standard: JESD 51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements, July 2000.

Cooling News

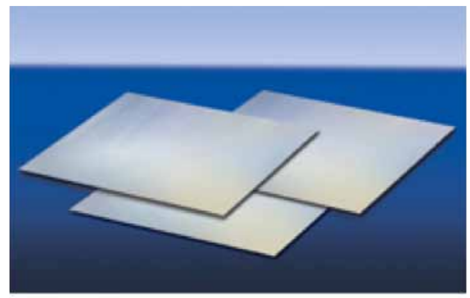
New Products, Services and Events from around the Industry

Thermal Gap Fillers Combine High Performance and Low Pricing

New TP-S30 thermal interface pads from MH&W International provide 3.0 W/mK of thermal conductivity between hot components and heat sinks at lower costs than competing gap filler materials. Pads of TP-S30 thermal gap fillers are soft and compliant, for easy compression and filling of air gaps between mounting surfaces, to optimize heat transfer. Applications for these gap fillers include: alternative energy, consumer electronics, telecommunications, power supplies, flat panel displays and portable electronics.

New Instrument System for Studying Air Flow and Air Temperature

The i-THERM 100 Airflow Measurement Test Station from Advanced Thermal Solutions includes a benchtop, laboratory-grade wind tunnel, controller and sensors to precisely manage the velocity and direction of airflow within its test environment. The system can be used to characterize airflow and to measure pressure drop across heat sinks. Studies can also be made on fans, fan trays, PCBs, ATCA cards and racks. The i-THERM 100 can be used with a thermocouple for heat management studies on CPUs or other components. The complete i-THERM 100 system provides a 15% savings over purchasing each instrument separately.



New Thermal Interface Silicone Putty

SARCON XR-Um-Al from Fujipoly is a new thermal gap filler. The material's putty-like consistency contributes to its low contact and thermal resistance while it maintains a thermal conductivity of 17 Watt/m-k. SARCON XR-Um-Al includes a thin aluminum carrier film for customer-friendly application. The low adhesion aluminum barrier enables users to remove the carrier film after installation with no pull-out effect. This thermal interface material is available in sheets up to 50 mm by 50 mm with thicknesses ranging from 0.2 mm to 0.5 mm.

Ellsworth Adhesives Releases New Line Card

Ellsworth Adhesives, a global distributor and value-added supplier of adhesives, sealants, coatings, encapsulants, tapes and dispensing equipment, has introduced its newly updated line card offering. The Ellsworth's line card provides a One Source comprehensive resource for customers looking for an inclusive list of material and equipment manufacturers. A complete list of value-added services is outlined, including technical support, custom labeling options, documentation expertise, certifications and custom formulating and packaging.

Forced Air-Cooled Chassis for Conduction-Cooled Modules

This XPand4200 1⁄2 ATR forced air-cooled chassis from Extreme Engineering Solutions meets rigorous MIL-STD-810 F/G standards at reduced height and length, while featuring the latest power-saving and performance-enhancing technology. Heat from the internal conduction-cooled modules is conducted to sidewall heat exchangers where it is dissipated to the ambient environment by forced-air cooling. Depending on processing requirements, the ruggedized XPand4200 can be populated with high-performance, low-power, conduction-cooled 3U VPX or cPCI modules.